REMARKS

This Amendment is submitted in response to the Examiner's Action dated October 28, 1998, having a shortened statutory period of response ending on January 28, 1999. In that action, the Examiner objected to the title as not being sufficiently descriptive. Claims 16 and 19 were rejected under 35 U.S.C. §112, second paragraph, regarding an insufficient antecedent basis for "said address tags." Claims 1-19 were rejected under 35 U.S.C. §103 as being unpatentable over Kalish in view of Lee.

Applicants have changed the title as suggested by the Examiner. Claim 16 has also been amended to cure the lack of antecedent basis.

With respect to the §103 rejections, Applicants would respectfully submit that Kalish and Lee do not render the present invention obvious, because neither of those references discloses or suggests a cache for a processing unit, wherein the cache provides at least two redundant cache directories, allowing simultaneous read operations using each of the cache directories, in a single clock cycle. Kalish is directed to fault tolerance for a cache memory of a processor. The problem addressed by Kalish relates to the desire to provide a high level of fault tolerance, without using components that are completely redundant and thus contribute to higher costs. In order to achieve fault tolerance without providing fully redundant caches, Kalish uses two cache controllers whose contents are mutually exclusive during normal operation (being confined to data having even or odd address tags, respectively) and, in the case of a failure of one of the cache controllers, using the remaining operational cache controller for all data (i.e., both even and odd address tags).

Applicants' invention, in contrast, uses at least two cache directories that are completely redundant. Kalish expressly eschews the use of redundant caches (see, e.g., column 3, lines 4-13). Because Kalish thus teaches away from the present invention, it is inappropriate to use it as a §103 reference, and one skilled in the art would not be motivated to combine Kalish in the manner

suggested in the Office Action. Moreover, Kalish still suffers from the same problems noted in the Background of Applicants' specification--the cache architecture does not allow two simultaneous read operations (i.e., in the same clock cycle) if both read operations are directed to even address tags, or if both read operations are directed to odd address tags. Depending upon the particular application running on the computer, this architecture could result in contending read operations more than 50% of the time. The partial benefit derived by Kalish when two operations are directed to even and odd address tags is a feature which is merely incidental to the more important goal of fault tolerance.

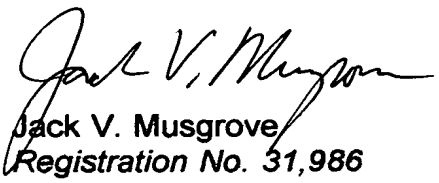
The Office Action acknowledges that Kalish does not have first and second cache directories, and ostensibly relies on Lee for this teaching. Lee, however, does not teach first and second cache directories which may be used to read first and second memory blocks, as Applicants have claimed. Lee provides a backside cache directory, and a frontside (bus agent) cache directory. The bus agent cache directory is primarily used to pass on a load instruction (read operation) to main memory in the event of a cache miss. The bus agent cache directory can also be used for snooping (coherency management), but is never used to allow access to the cache entry array (data ram 16). Because Lee does not provide read ports for two or more cache directories, one skilled in the art would not be motivated to combine Lee as suggested in the Office Action. Indeed, the proposed combination of Kalish and Lee still would not result in the claimed invention since a combination of Kalish and Lee would only lead to a cache architecture having an external directory segmented into even and odd portions, but that was still unusable for directly accessing the cache entry array (i.e., in the same clock cycle).

Notwithstanding the foregoing, Applicants have amended Claim 1 to clarify that the first and second cache directories are redundant, such that a given address tag is written to a specific line of the first directory and to a specific line of the second directory that corresponds to the specific line of the first directory, and that the first and second memory blocks are read in a single

clock cycle of the processor. These amendments serve to further distinguish Applicants' invention from the cited references. Claims 2, 5 and 11-13 have accordingly been deleted, and the dependencies of Claims 6 and 14-16 have been amended for consistency. For all of the foregoing reasons, Applicants respectfully request reconsideration of the §103 rejections.

Applicants have diligently responded to the Office Action by amending claims, deleting others, and by pointing out with particularity how the claims as presented patentably define the invention over the prior art of record. A Notice of Allowance of the claims now pending is respectfully requested.

Respectfully submitted,



Jack V. Musgrove
Registration No. 31,986
For FELSMAN, BRADLEY, GUNTER
& DILLON, LLP
Suite 350, Lakewood on the Park
7600B North Capital of Texas Highway
Austin, Texas 78731
512-343-6116
ATTORNEY FOR APPLICANTS